REMARKS

The Office Action mailed December 23, 2004, has been received and reviewed. Claims 1 through 20 are currently pending in the application. Claims 7, 9 and 10 stand rejected. Claim 8 has been objected to as being dependent upon a rejected base claim, but the indication of allowable subject matter in such claim is noted with appreciation. Applicants respectfully request reconsideration of the application in view of the arguments set forth hereinbelow.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,286,656 to Keown et al.

Claims 7, 9 and 10 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Keown et al. (U.S. Patent No. 5,286,656). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner cites Keown as "disclosing a semiconductor die assembly (figure 4), comprising: a semiconductor die having a plurality of bonding pads (DBP5); a lead frame having a plurality of conductive leads (Figure 4), each conductive lead being electrically coupled at spaced locations on the conductive lead to at least two bond pads of the plurality of bond pads (Figures 2-4, a lead frame TNMOS coupled at least two bond pads), and a wire bond coupling each conductive lead at the spaced locations thereon to one of the at least two bond pads of plurality of bond pads (Figures 2-4), and wherein each conductive lead includes a severance region [configured] to facilitate separation thereof into at least two mutually electrically isolated conductive elements." (Office Action, pages 2 and 3). Applicants respectfully traverse this rejection.

Keown is directed to a "method of fabricating and testing integrated circuit (IC) dies on a wafer and a new wafer structure for individualized *prepackage testing* of the IC dies on the wafer before scribing and packaging." (Col. 1, lines 9-12, emphasis added). Additionally, Keown

states that the invention "provides individualized *prepackage testing* of AC performance of a selected sensitive AC parameter for all dies on the wafer at the wafer level stage during DC parametric testing." (*Id.* lines 9-15, emphasis added).

In providing a wafer with individualized prepackage testing, Keown teaches that a test NMOS transistor (labeled TNMOS) includes a gate node (G) which is coupled to a drain node (D). According to Keown, the "gate and drain nodes G, D, are coupled to a first test bond pad or dedicated bond pad DBP1 for applying or forcing a test voltage during DC parametric testing." (Col. 4, lines 60-67). Additionally, the source node (S) of the TNMOS is coupled to a ground rail (GND) bond pad of the IC die (10). (*Id.*, col. 4, line 67 – col. 5, line 2).

Thus, Keown teaches an NMOS *transistor*, as part of each IC die's circuitry, being coupled between two different bond pads thereof. Applicants respectfully submit that the internal circuitry taught by Keown clearly does not read on the "lead frame having a plurality of conductive leads" recited by claim 7 of the presently claimed invention. Likewise, Applicants submit that the TNMOS transistor integrated into Keown's circuitry is clearly not a "conductive lead" of a lead frame.

As such, Applicants respectfully submit that claim 7 is clearly allowable over Keown and respectfully request the same. Applicants further submit that claims 9 and 10 are also allowable as being dependent from an allowable base claim as well as for the additional patentable subject matter introduced thereby.

With respect to claim 9, Applicants submit that, even if the internal circuitry of Keown were to be considered a lead frame and the TNMOS transistor of Keown were to be considered a conductive lead of the lead frame (and Applicants maintain their position to the contrary), that Keown does not teach a wire bond coupling the TNMOS transistor and the two bond pads.

With respect to claim 10, While the Examiner has cited Keown as teaching that each conductive lead has a severance region configured to facilitate separation thereof into at least two mutually electrically isolated conductive elements, the Examiner does not point to any specific teachings of Keown and Applicants fail to find such subject matter being taught by Keown.

Applicants, therefore, respectfully request reconsideration and allowance of claim claims 7, 9 and 10.

Allowable Subject Matter

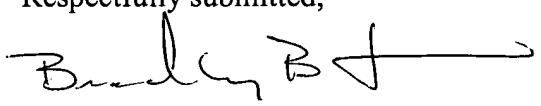
Claim 8 stands objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form.

As noted hereinabove, Applicants submit that claim 7 is allowable over the reference relied upon by the Examiner. As such, Applicants submit that claim 8 is in condition for allowance and respectfully request the same.

CONCLUSION

Claims 1 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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Date: March 22, 2005
BBJ/djp:lmh
Document in ProLaw